

FIG.1A



FIG.1B

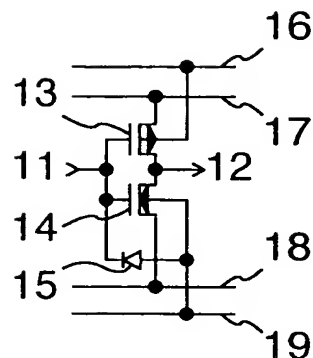


FIG.1C

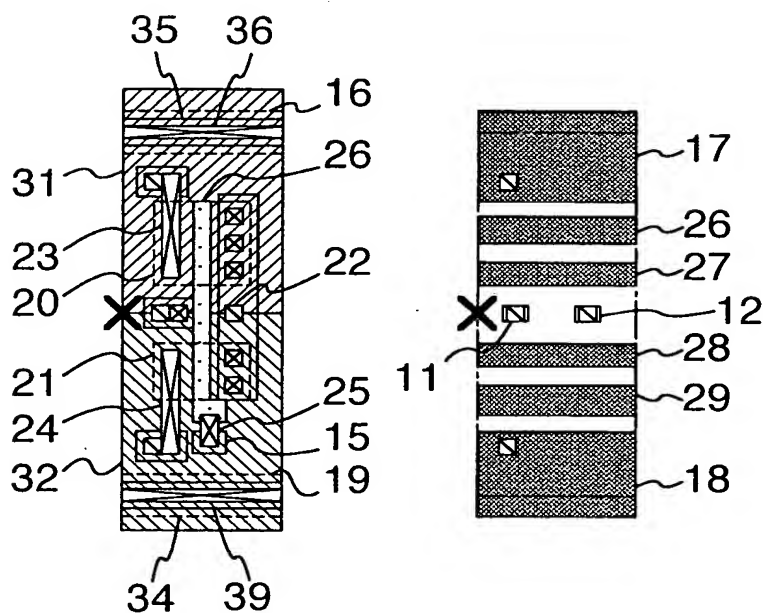


FIG.1D

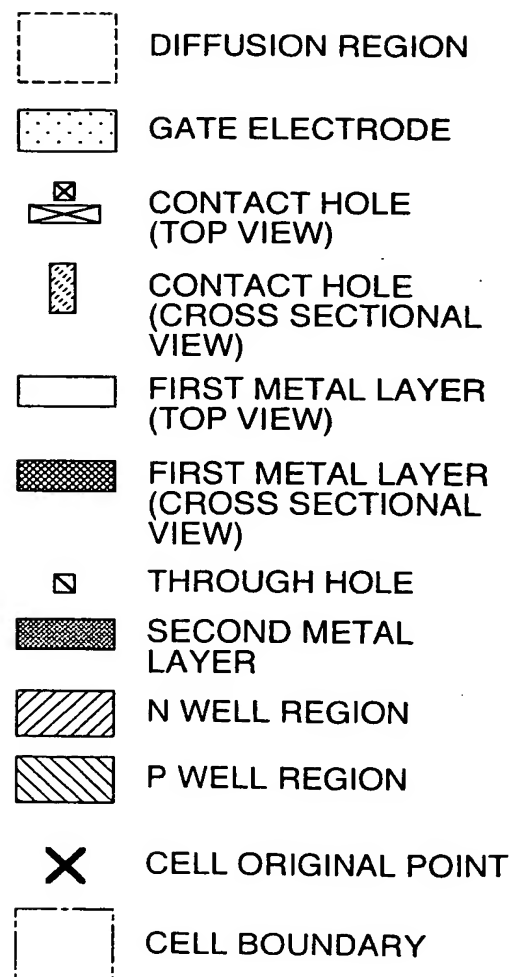
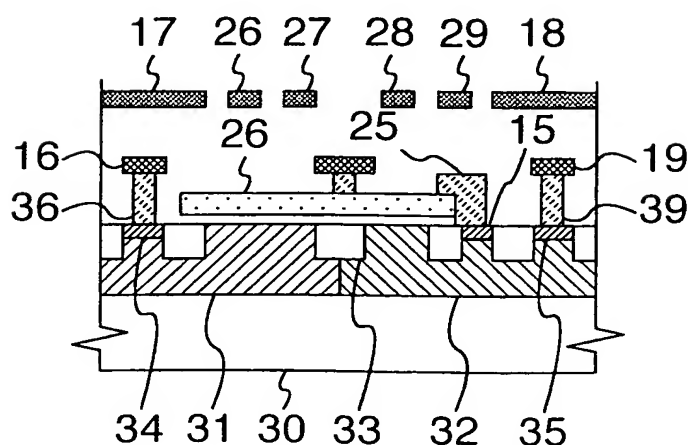


FIG.2A

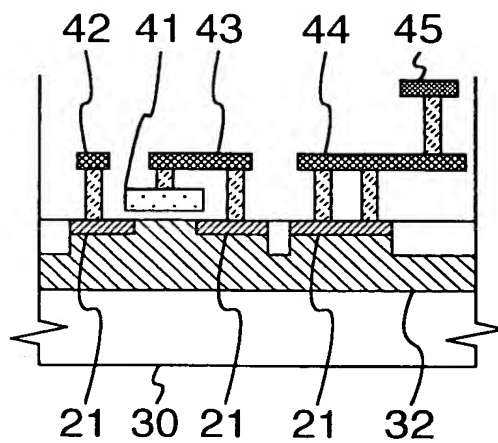


FIG.2B

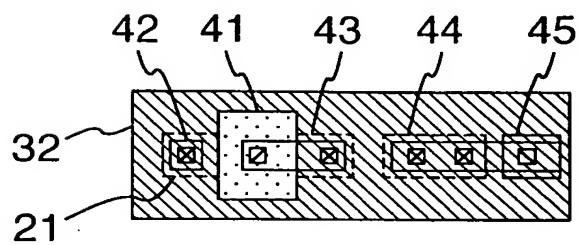


FIG.2C

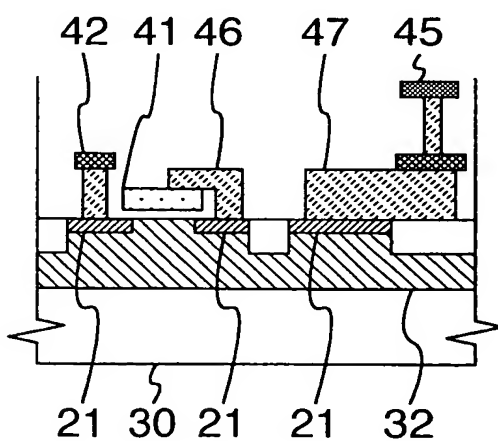


FIG.2D

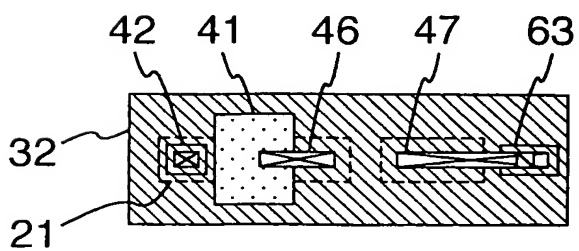


FIG.3A

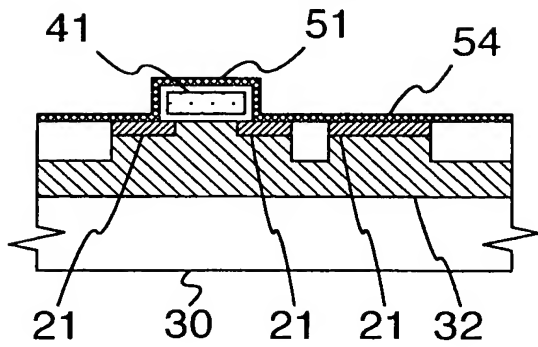


FIG.3E

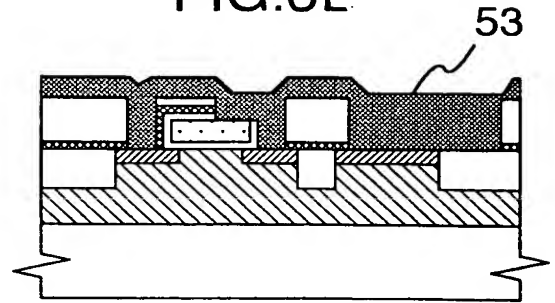


FIG.3B

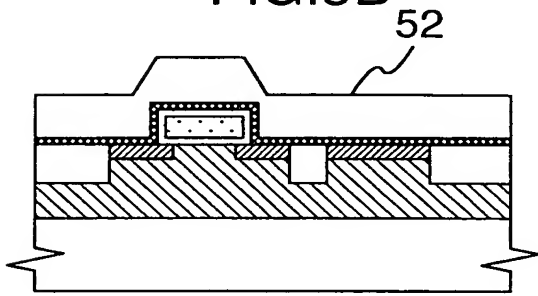


FIG.3F

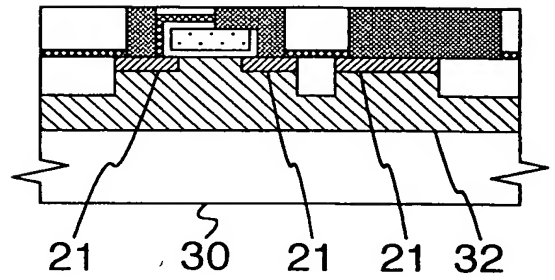


FIG.3C

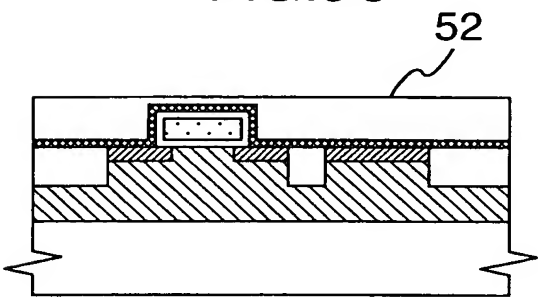


FIG.3G

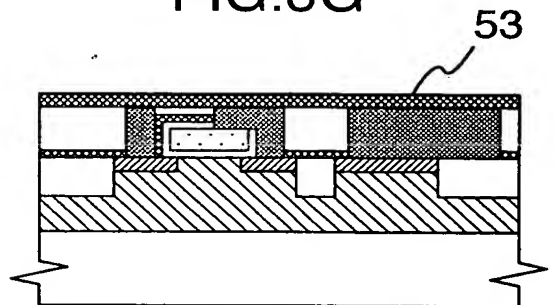


FIG.3D

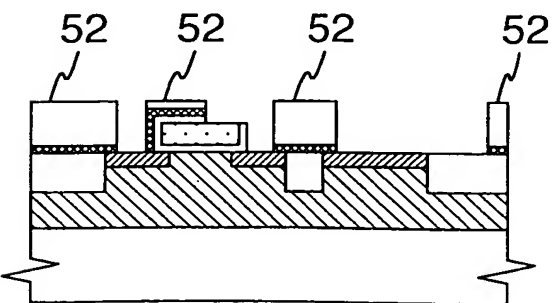


FIG.3H

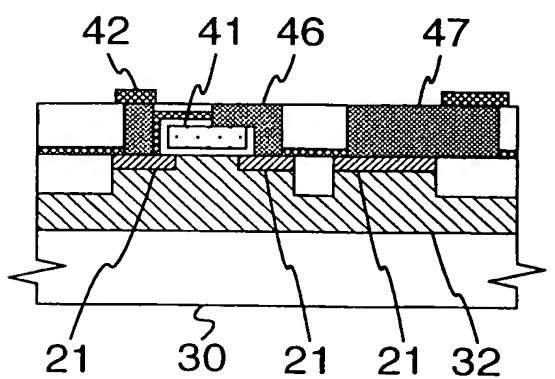


FIG.4A

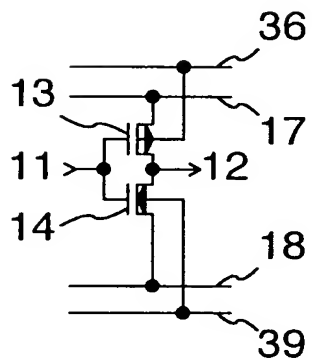


FIG.4B

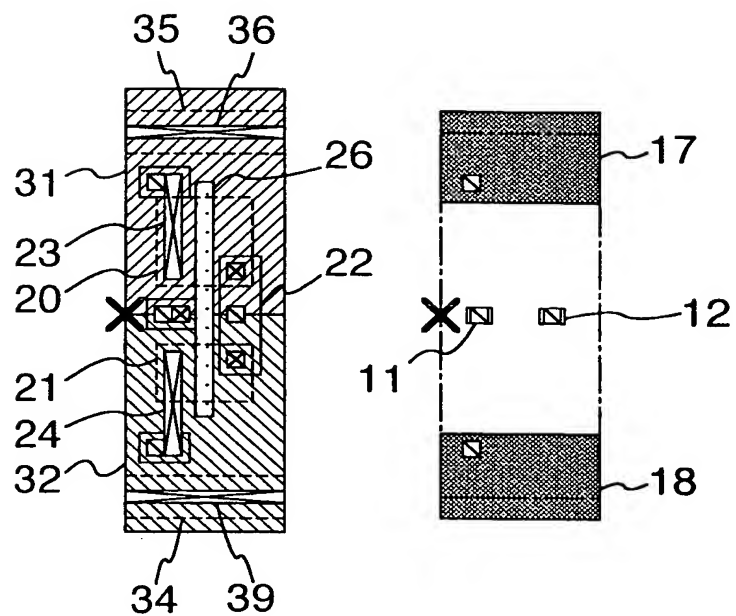


FIG.4C

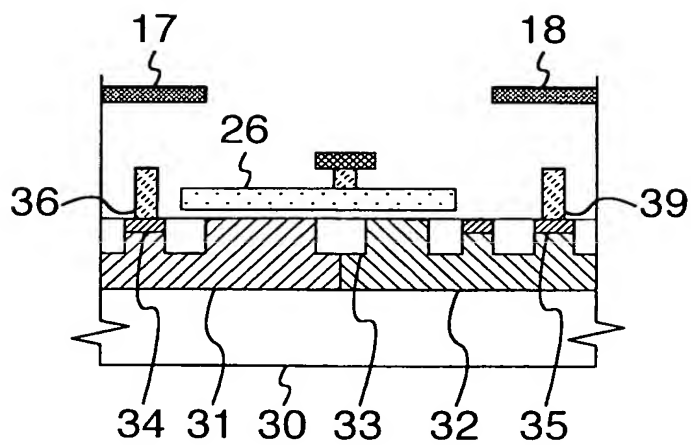


FIG.4D

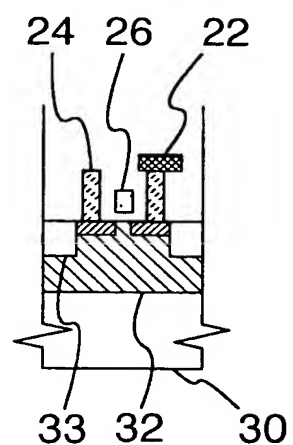


FIG.5A

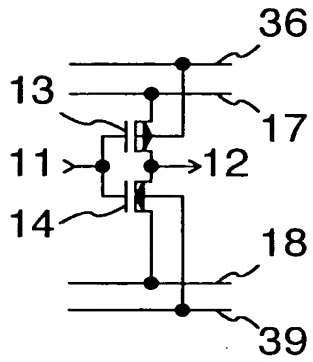


FIG.5B

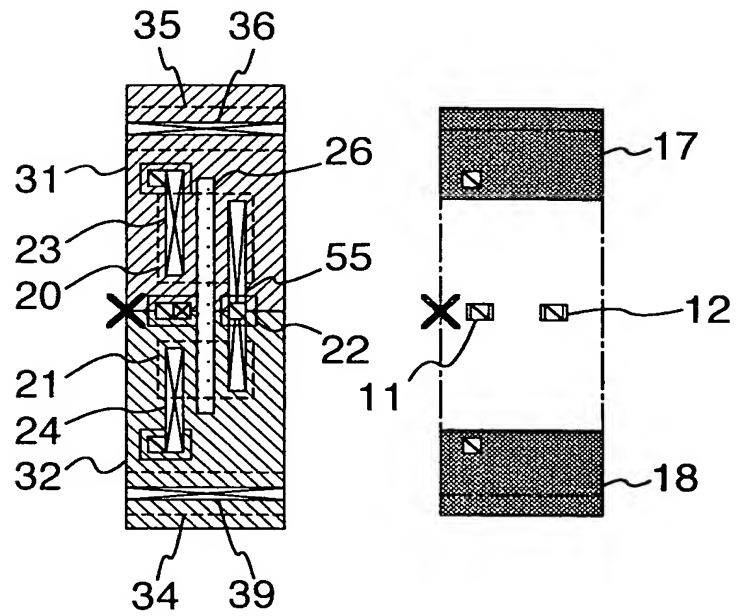


FIG.5C

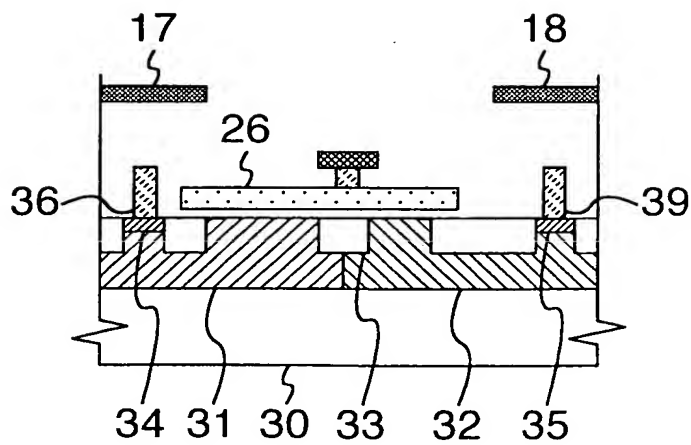


FIG.5D

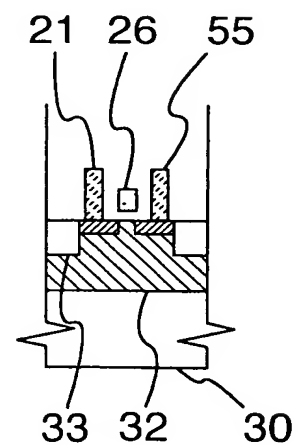


FIG.6A

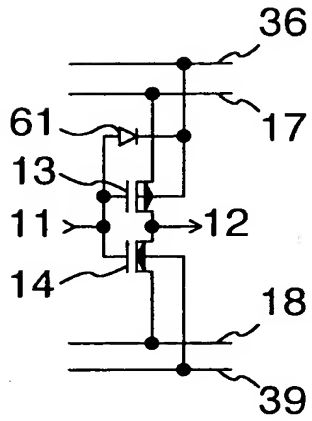


FIG.6B

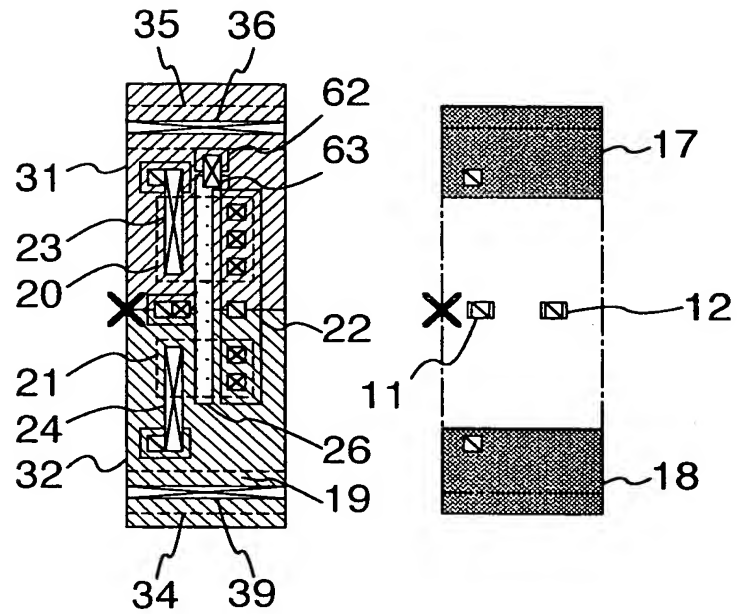


FIG.6C

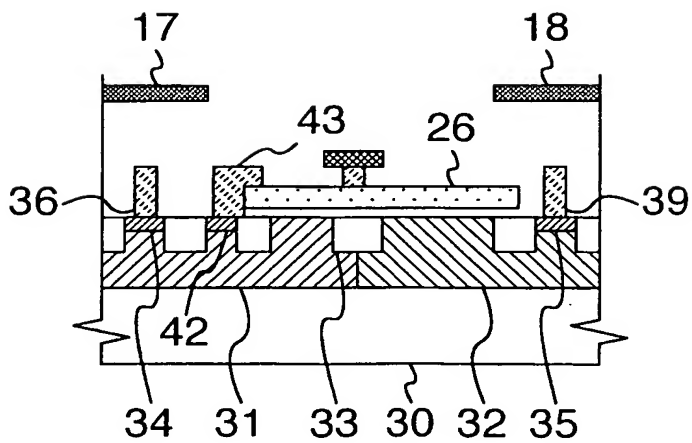


FIG.6D

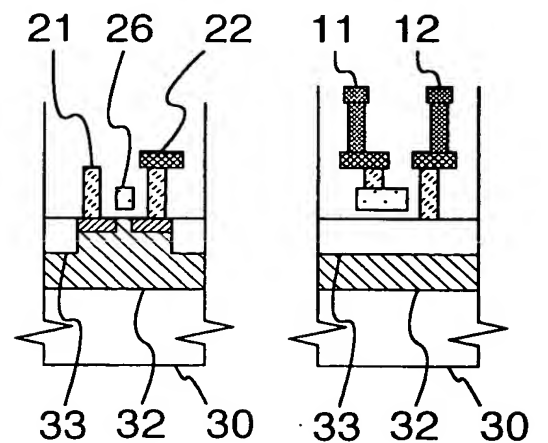


Figure 1 consists of two diagrams. The left diagram is a cross-sectional view of a semiconductor device. It shows a substrate 16 with a top layer 35 and 36, a central region 20 with a p-n junction 21, and a bottom layer 34 and 39. The right diagram is a plan view of the device, showing a rectangular structure with a central region 11, a top layer 17, and a bottom layer 18. A dashed line 12 indicates a boundary or interface.

[illegible]

A cross-sectional view of a semiconductor device. It features a central gate structure (26) on a substrate (30). The gate structure includes a gate dielectric (21) and a gate electrode (22). The substrate (30) is divided into a central region (32) and side regions (33). The side regions (33) are doped with a different material than the central region (32), as indicated by the different hatching patterns.

FIG.8A

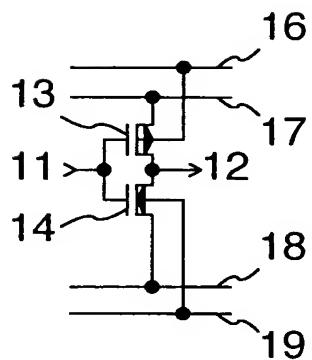


FIG.8B

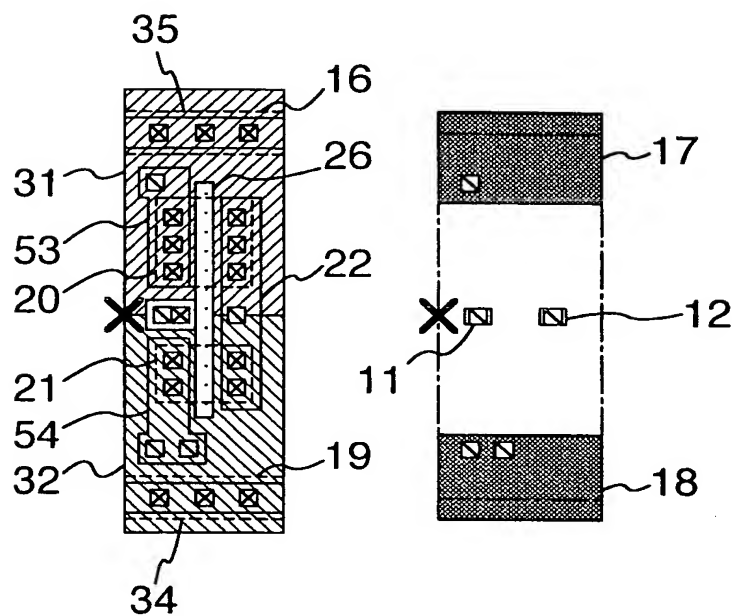
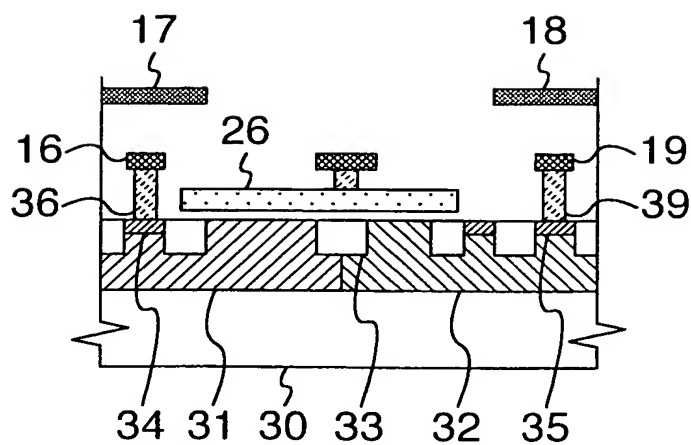


FIG.8C



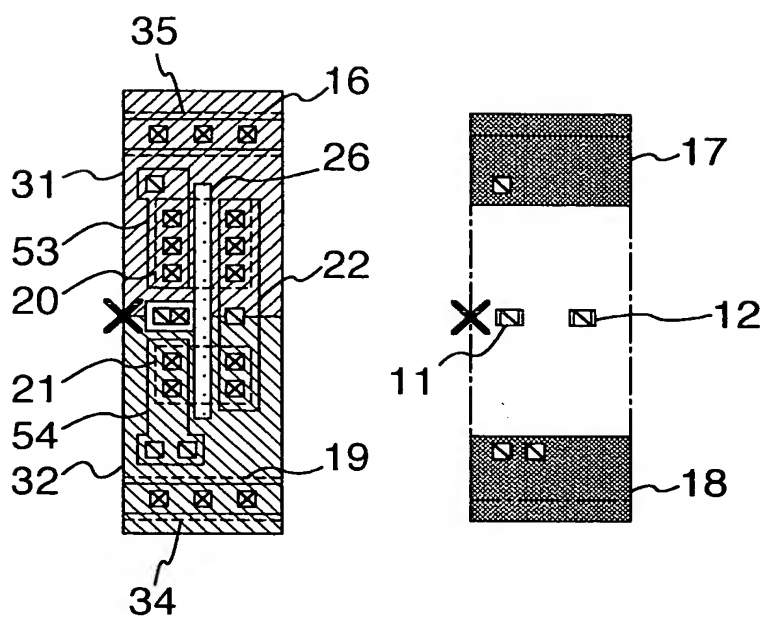


FIG.10A

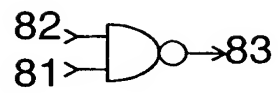


FIG.10B

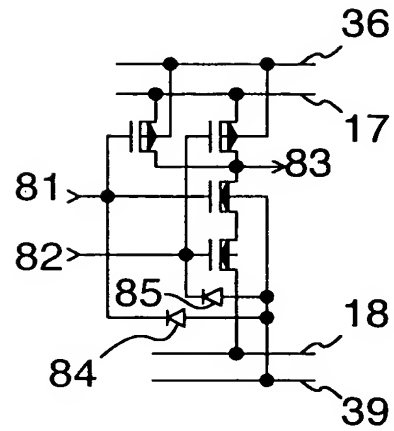
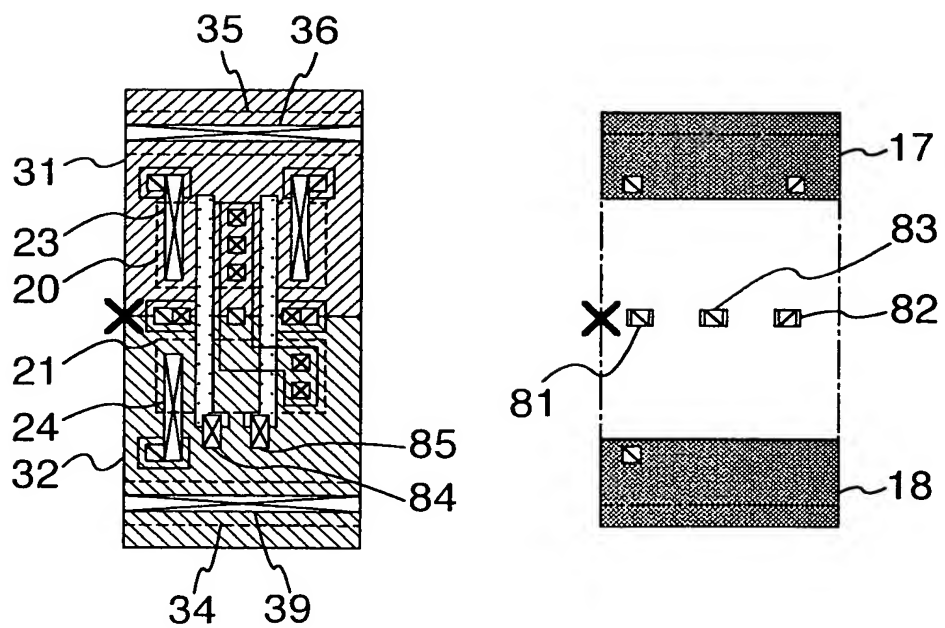


FIG.10C



[illegible]

Figure 1 is a schematic diagram of a semiconductor device structure. The diagram shows a cross-section of a device with various layers and regions. Labels 36, 17, 18, and 39 indicate different layers or regions. Labels 81, 83, and 82 point to specific features. A large 'X' is marked in the center. The right side of the diagram shows a series of vertical bars representing different electrical connections: Vss, Vbn, Cbn, Cbp, Vbp, and Vcc.

FIG.12A

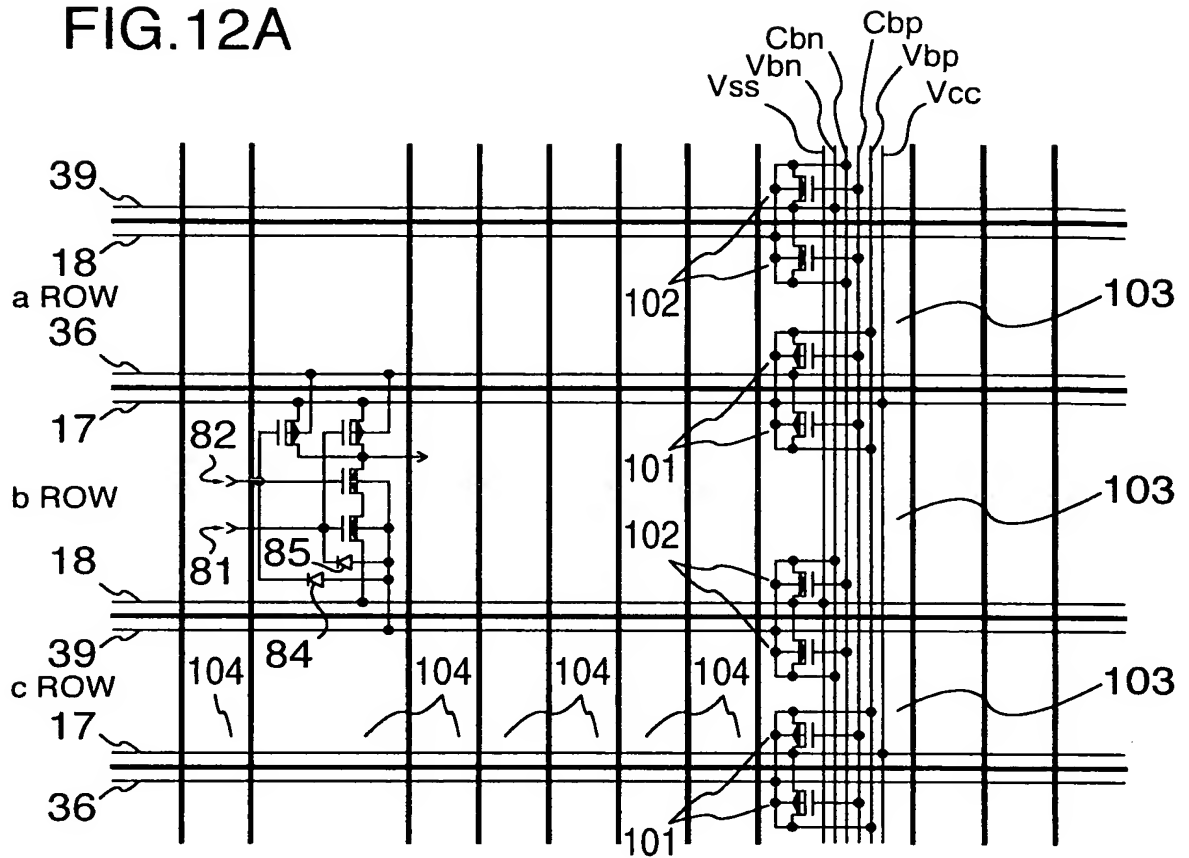


FIG.12B

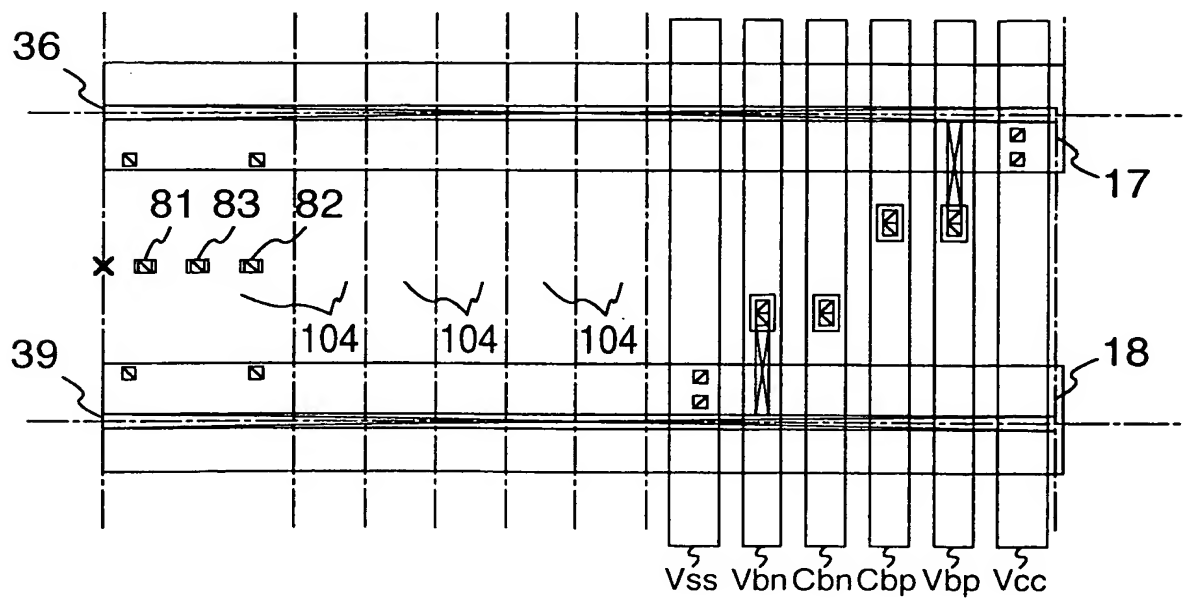


FIG.13A

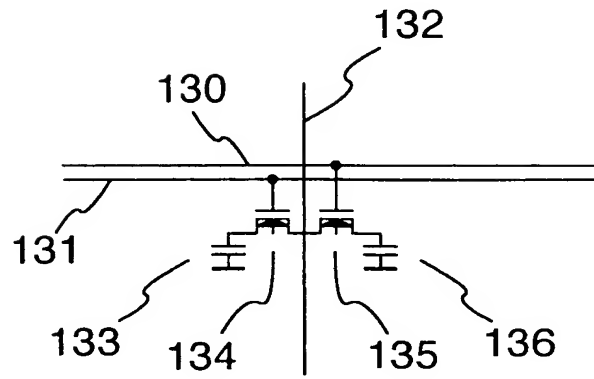


FIG.13B

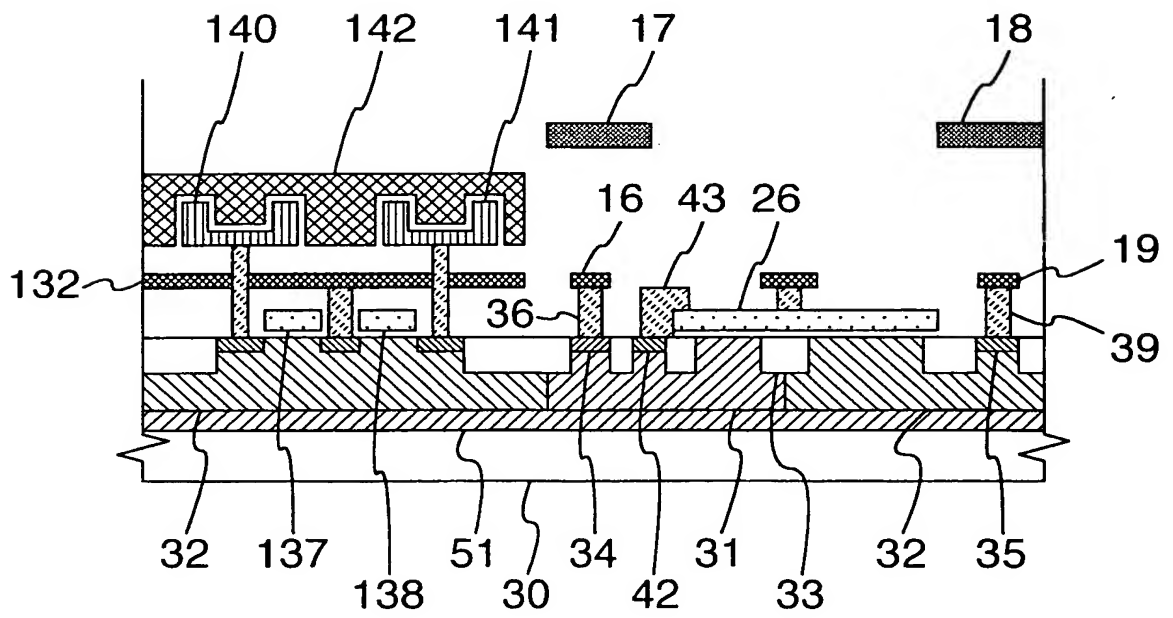


FIG.14

